What is claimed is:

1. A refresh clock generator, comprising:

a first temperature adaptive current generating circuit for outputting a first current in proportion to temperature variation;

a second temperature adaptive current generating circuit for outputting a second current in inverse proportion to temperature variation; and

a bias voltage generator for receiving the first and second currents and outputting first and second bias voltages corresponding to a third current that subtracts the second current from the first current.

2. The refresh clock generator as recited in claim 1, further comprising:

a clock generator for receiving the first and second bias voltages and generating a refresh clock signal having a frequency which is controlled or adjusted based on the first and the second bias voltage.

3. The refresh clock generator as recited in claim 2, further comprising:

a subsidiary bias voltage generator for receiving the first current and outputting first and second subsidiary bias voltages to the clock generator in response to the first current.

4. The refresh clock generator as recited in claim 3, wherein the bias voltage generator includes:

a first current mirror device for outputting the third current mirrored from the second current;

a second current mirror device having a first MOS transistor for outputting a fifth current mirrored from a forth current which subtracts the third current from the first current; and

a second MOS transistor diode-connected between a supply voltage and the second current mirror device for outputting the fifth current to the second current mirror device,

wherein gate of the second MOS transistor outputs a first bias voltage and gate of the first MOS transistor outputs a second bias voltage.

5. The refresh clock generator as recited in claim 4, wherein the clock generator including several inverters is operated by a first operating current corresponding to the first and second bias voltages and a second operating current corresponding to the first and second subsidiary bias voltages and outputs the refresh clock signal having a frequency which is controlled or adjusted based on the first and the second operating currents.

6. The refresh clock generator as recited in claim 5, wherein the inverter includes:

a third MOS transistor for forming a current-mirror device with the second MOS transistor in the bias voltage generator, source of the third MOS transistor being connected to a supply voltage and gate of the third MOS transistor being connected to gate of the second MOS transistor;

a forth MOS transistor for forming a current-mirror device with the first MOS transistor that constitutes the second current mirror device in the bias voltage generator, source of the forth MOS transistor being connected to a ground voltage and gate of the forth MOS transistor being connected to gate of the first MOS transistor;

a fifth MOS transistor for receiving an output of the subsidiary bias voltage generator at gate, source of the fifth MOS transistor being connected to the supply voltage;

a sixth MOS transistor for receiving another output of the subsidiary bias voltage generator at gate, source of sixth MOS transistor being connected to the ground voltage;

a seventh MOS transistor of which source is connected to the drains of the third and the fifth MOS transistors; and

a eighth MOS transistor of which source is connected to the drains of the forth and the sixth MOS transistor,

wherein gates of the seventh and the eighth MOS transistor is coupled to a inputted signal and the seventh and eighth MOS transistor output a inversed signal through a node between drain of the seventh MOS transistor and drain of the eighth MOS transistor.

7. The refresh clock generator as recited in claim 6, the fifth current is made by mirroring a current which multiplies the forth current by α.

8. The refresh clock generator as recited in claim 7, the first temperature adaptive current generating circuit includes:

a first PMOS transistor diode-connected by connecting source to gate, source of first PMOS transistor being connected to the supply voltage;

a second PMOS transistor for forming current mirror with the first PMOS transistor, source of the second PMOS transistor being connected to the supply voltage and gate of the second PMOS transistor being connected to the gate of the first PMOS transistor;

a first NMOS transistor diode-connected by connecting gate and drain, the drain of the first NMOS transistor being connected to the drain of the second PMOS transistor;

a second NMOS transistor for forming current-mirror with the first NMOS transistor, drain of the second NMOS transistor being connected to the drain of the first PMOS transistor and gate of the second NMOS transistor being connected to the gate of the first NMOS transistor;

a first diode having a plus input connected to the source of the first NMOS transistor and a minus input connected to the ground voltage;

a first resistor connected to the source of the second

NMOS transistor;

a second diode having a plus input connected to the resistor and a minus input connected to the ground voltage; and

a third PMOS transistor for forming a current mirror device with the first PMOS transistor, source of the third PMOS transistor being connected to the supply voltage and gate of the third PMOS transistor being connected to the gate of the first PMOS transistor,

wherein the first current is mirrored by the third PMOS transistor.

9. The refresh clock generator as recited in claim 8, the second temperature adaptive current generating circuit includes:

a forth PMOS transistor diode-connected by connecting source to gate, source of the forth PMOS transistor being connected to the supply voltage;

a fifth PMOS transistor for forming current mirror with the forth PMOS transistor, source of the fifth PMOS transistor being connected to the supply voltage and gate of the fifth PMOS transistor being connected to the gate of the first PMOS transistor;

a third NMOS transistor diode-connected by connecting gate and drain, the drain of the third NMOS transistor being connected to the drain of the fifth PMOS transistor;

a forth NMOS transistor for forming a current mirror

device with the third NMOS transistor, drain of the forth NMOS transistor being connected to the drain of the forth PMOS transistor and gate of the forth NMOS transistor being connected to the gate of the third NMOS transistor;

a third diode having a plus input connected to the third NMOS transistor and a minus input connected to the ground voltage;

a second resistor coupled between the source of the forth NMOS transistor and the ground voltage; and

a sixth PMOS transistor for forming a current mirror device with the forth PMOS transistor, source of sixth PMOS transistor being connected to the supply voltage and gate of sixth PMOS transistor being connected to the gate of the forth PMOS transistor,

wherein the second current is mirrored by the sixth PMOS transistor.

10. The refresh clock generator as recited in claim 9, the subsidiary bias voltage generator includes:

a seventh PMOS transistor for outputting a sixth current mirrored from the first current and forming a current mirror device with the first PMOS transistor, source of the seventh PMOS transistor being connected to the supply voltage and gate of the seventh PMOS transistor being connected to the gate of the first PMOS transistor;

a third current mirror device having a fifth MOS transistor for outputting a seventh current mirrored from the

sixth current; and

a sixth MOS transistor diode-connected by connecting source to gate for outputting the seventh current to the third current mirror device, source of sixth MOS transistor being connected to the supply voltage,

wherein the gate of the fifth MOS transistor outputs a the first subsidiary bias voltage and the gate of the third MOS transistor outputs a second subsidiary bias voltage.

11. A semiconductor device having a refresh operation unit for performing a refresh operation in response to a refresh clock, comprising:

a first temperature adaptive current generating circuit for outputting a first current in proportion to temperature variation;

a second temperature adaptive current generating circuit for outputting a second current in inverse proportion to temperature variation; and

a bias voltage generator for receiving the first and second currents and outputting first and second bias voltages corresponding to a third current that subtracts the second current from the first current.

12. The semiconductor device of claim 11, further comprising:

a clock generator for receiving the first and second bias voltages and generating a refresh clock signal having a

frequency which is controlled or adjusted based on the first and the second bias voltage.

13. The semiconductor device of claim 12, further comprising:

a subsidiary bias voltage generator for receiving the first current and outputting first and second subsidiary bias voltages to the clock generator in response to the first current.

14. The semiconductor device of claim 13, wherein the bias voltage generator includes:

a first current mirror device for outputting the third current mirrored from the second current;

a second current mirror device having a first MOS transistor for outputting a fifth current mirrored from a forth current which subtracts the third current from the first current; and

a second MOS transistor diode-connected between a supply voltage and the second current mirror device for outputting the fifth current to the second current mirror device,

wherein gate of the second MOS transistor outputs a first bias voltage and gate of the first MOS transistor outputs a second bias voltage.

15. The semiconductor device of claim 14, wherein the clock generator including several inverters is operated by a

first operating current corresponding to the first and second bias voltages and a second operating current corresponding to the first and second subsidiary bias voltages and outputs the refresh clock signal having a frequency which is controlled or adjusted based on the first and the second operating currents.

16. The semiconductor device of claim 15, wherein the inverter includes:

a third MOS transistor for forming a current-mirror device with the second MOS transistor in the bias voltage generator, source of the third MOS transistor being connected to a supply voltage and gate of the third MOS transistor being connected to gate of the second MOS transistor;

a forth MOS transistor for forming a current-mirror device with the first MOS transistor that constitutes the second current mirror device in the bias voltage generator, source of the forth MOS transistor being connected to a ground voltage and gate of the forth MOS transistor being connected to gate of the first MOS transistor;

a fifth MOS transistor for receiving an output of the subsidiary bias voltage generator at gate, source of the fifth MOS transistor being connected to the supply voltage;

a sixth MOS transistor for receiving another output of the subsidiary bias voltage generator at gate, source of sixth MOS transistor being connected to the ground voltage;

a seventh MOS transistor of which source is connected to the drains of the third and the fifth MOS transistors; and

a eighth MOS transistor of which source is connected to the drains of the forth and the sixth MOS transistor,

wherein gates of the seventh and the eighth MOS transistor is coupled to a inputted signal and the seventh and eighth MOS transistor output a inversed signal through a node between drain of the seventh MOS transistor and drain of the eighth MOS transistor.

17. The semiconductor device of claim 16, the fifth current is made by mirroring a current which multiplies the forth current by α.

18. The semiconductor device of claim 17, the first temperature adaptive current generating circuit includes:

a first PMOS transistor diode-connected by connecting source to gate, source of first PMOS transistor being connected to the supply voltage;

a second PMOS transistor for forming current mirror with the first PMOS transistor, source of the second PMOS transistor being connected to the supply voltage and gate of the second PMOS transistor being connected to the gate of the first PMOS transistor;

a first NMOS transistor diode-connected by connecting gate and drain, the drain of the first NMOS transistor being connected to the drain of the second PMOS transistor;

a second NMOS transistor for forming current-mirror with the first NMOS transistor, drain of the second NMOS transistor

being connected to the drain of the first PMOS transistor and gate of the second NMOS transistor being connected to the gate of the first NMOS transistor;

a first diode having a plus input connected to the source of the first NMOS transistor and a minus input connected to the ground voltage;

a first resistor connected to the source of the second NMOS transistor;

a second diode having a plus input connected to the resistor and a minus input connected to the ground voltage; and

a third PMOS transistor for forming a current mirror device with the first PMOS transistor, source of the third PMOS transistor being connected to the supply voltage and gate of the third PMOS transistor being connected to the gate of the first PMOS transistor,

wherein the first current is mirrored by the third PMOS transistor.

19. The semiconductor device of claim 18, the second temperature adaptive current generating circuit includes:

a forth PMOS transistor diode-connected by connecting source to gate, source of the forth PMOS transistor being connected to the supply voltage;

a fifth PMOS transistor for forming current mirror with the forth PMOS transistor, source of the fifth PMOS transistor being connected to the supply voltage and gate of the fifth

PMOS transistor being connected to the gate of the first PMOS transistor;

a third NMOS transistor diode-connected by connecting gate and drain, the drain of the third NMOS transistor being connected to the drain of the fifth PMOS transistor;

a forth NMOS transistor for forming a current mirror device with the third NMOS transistor, drain of the forth NMOS transistor being connected to the drain of the forth PMOS transistor and gate of the forth NMOS transistor being connected to the gate of the third NMOS transistor;

a third diode having a plus input connected to the third NMOS transistor and a minus input connected to the ground voltage;

a second resistor coupled between the source of the forth NMOS transistor and the ground voltage; and

a sixth PMOS transistor for forming a current mirror device with the forth PMOS transistor, source of sixth PMOS transistor being connected to the supply voltage and gate of sixth PMOS transistor being connected to the gate of the forth PMOS transistor,

wherein the second current is mirrored by the sixth PMOS transistor.

20. The semiconductor device of claim 19, the subsidiary bias voltage generator includes:

a seventh PMOS transistor for outputting a sixth current mirrored from the first current and forming a current mirror

device with the first PMOS transistor, source of the seventh PMOS transistor being connected to the supply voltage and gate of the seventh PMOS transistor being connected to the gate of the first PMOS transistor;

a third current mirror device having a fifth MOS transistor for outputting a seventh current mirrored from the sixth current; and

a sixth MOS transistor diode-connected by connecting source to gate for outputting the seventh current to the third current mirror device, source of sixth MOS transistor being connected to the supply voltage,

wherein the gate of the fifth MOS transistor outputs a the first subsidiary bias voltage and the gate of the third MOS transistor outputs a second subsidiary bias voltage.